

Special Issue of First International Conference on Innovations in Engineering Sciences (ICIES 2020) Improved Performance of M-Ary PSK Modulation over AWGN Channel Using Channel Coding Technique

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Abstract

Spectral efficiency improvement with guaranteed communication consistency using channel coding techniques is the direction in which communication systems evolves. This paper presents M-ary PSK modulation performance over AWGN channel for higher M values. In this paper we simulate the performance of M-ary PSK modulation for higher orders of modulation applying irregular LDPC channel coding technique and obtain improved SNR as compared to uncoded M-ary Phase Shift Keying for M values varying from 4 to 4096.

.Keywords: M-PSK; LDPC; AWGN; SNR.

1. Introduction

Higher order modulations are a choice of digital communication systems designers to achieve higher spectral efficiency[1]. The commonly used higher order modulations are M-ary phase-shift keying(M-PSK), M-ary quadrature amplitude (M-QAM) and M-ary amplitude and phase-shift (M-APSK) keying. Gallager discovered LDPC (Low Density Parity-Check Code) in 1962, based on linear block codes described by the parity check matrix[2]. MacKay and Neal rediscovered and proved in 1996 that LDPC codes have good performance that approaches the Shannon limit [3, 4]. An LDPC code is a linear block code having the parity check matrix with low density of 1's. LDPC codes are called regular if its parity check matrix has the wc Number 1 in each column and wr = wc(n / m) 1 in each row, where wc < <m is used. The function R = k / n is also

represented by $R=1-w_c/w_r$. The LDPC code is called irregular if the number of 1's in each row or column is not constant.

The graphical representation of LDPC codes is done with tanner graph or bipartite graph. In this graph, there are 2 nodes called check node(cnode)s and variable node(v-node)s and edges which make connection between variable nodes and check nodes. The rule for drawing the tanner graph: check node j is connected to variable node i whenever element h_{ii} in H is a 1. The m-rows of H represent the m c-node connections and the n columns of Η specify the n v-node connections[6,7,8,9,10]. Most of the studies on LDPC codes, considers BPSK modulation. In order to meet the demands of telecommunication industries in terms of higher order modulation and high spectral efficiency, BPSK cannot reach the practical requirements [5,11,12]. Literatures available on LDPC Codes seldom include the LDPC encoding and decoding theory and

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mechanism under higher order modulation. In this paper therefore the detailed research on LDPC encoding and decoding under higher order modulation.

2. Experimental Method

The LDPC codes are linear block codes with minimal 1s H, long block length matrices that can reach near Shannon limit performance.

The matrix Parity-check is defined by N binary valued matrix as a sparse (N - K), where N is the length of the output codeword vector, and is within the range (0, 231). K is the length of the message uncoded, which must be less than N. The Galois field of order 2,gf(2) must be satisfied by the last column (N - K) in the matrix check-parity. In the coding is used the parity-check matrix of size 32,400-by-64,800 which corresponds to an irregular LDPC code with the structure below. is used in the coding.

Row	Number of 1s per Row
1	6
2 to 32400	7
Column	Number of 1s per
	Column
1 to 12960	8
12961-	3
32400	

The lower triangular matrix is formed by columns from 32,401 to 64,800. To solve the parity-check equation, forward or backward substitution method is used if the triangular matrix is formed by the (N-K) last columns of parity check matrix otherwise matrix inversion method is used. The properties of the encoder/decoder and modulator/demodulator are given below.

LDPC Encoder Properties:

ParityCheckMatrix: [32400×64800 logical]

LDPC Decoder Properties:

ParityCheckMatrix: [32400×64800 logical] OutputValue: 'Information part' DecisionMethod: 'Hard decision' MaximumIterationCount: 50 IterationTerminationCondition: 'Maximum iteration count' NumIterationsOutputPort: false FinalParityChecksOutputPort: false **Modulator properties:** PSK modulation order varying from M=4 to M=4096. Phase offset: 0.3927 BitInput: true SymbolMapping: 'Gray' OutputDataType: 'double'

Demodulator Properties:

PSK modulation order varying from M=4 to M=4096. PhaseOffset: 0.3927 BitOutput: true SymbolMapping: 'Gray' DecisionMethod: 'Approximate log-likelihood ratio' VarianceSource: 'Property' Variance: 1

3. Results And Discussion

The simulation graphs below depict the performance of M-ary PSK modulation with and without the irregular LDPC channel coding in terms of Signal to Noise Ratio. The SNR is found to be 1dB, 2.3dB, 7dB, 9dB, 14.5dB, 15dB, 22dB, 25 dB, 28dB, 35dB for QPSK, 8PSK, 16PSK, 32PSK, 64PSK, 256PSK, 512PSK, 1024PSK, 4096PSK respectively.



Fig.1:Uncoded and LDPC coded QPSK



Fig.2:Uncoded and LDPC coded 8PSK



Fig.3:Uncoded and LDPC coded 16PSK



Fig.4:Uncoded and LDPC coded 32PSK



Fig.5:Uncoded and LDPC coded 64PSK



Fig.6:Uncoded and LDPC coded 128PSK



Fig.7:Uncoded and LDPC coded 256PSK



Fig.8:Uncoded and LDPC coded 512PSK



Fig.9:Uncoded and LDPC coded 1024PSK



Fig.10:Uncoded and LDPC coded 4096PSK

Conclusion

The simulation of M-ary PSK modulation with and Without LDPC channel coding was carried out using MATLAB too. The comparison of uncoded PSK modulation and LDPC coded PSK modulation from M=4 to M=4096 is plotted and observed that LDPC coded M-ary PSK modulation will provide better SNR characteristics as compared to uncoded M-ary PSK. The study of Mary PSK is ignored by the researchers due to its poor performance for higher order modulation. In this study an effort is made to analyze the performance with the efficient channel codes such as LDPC. We conclude that efficient channel coding techniques can improve the performance of M-ary PSK modulation.

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